**ENERGY-EFFICIENT MEMORY-CENTRIC ACCELERATOR DESIGN FOR MOBILE/EDGE-BASED AI INFERENC**

PO-TSANG HUANG
NATIONAL CHIAO TUNG UNIV., TAIWAN
9:00-10:30AM | SEPT. 8

**Abstract:** Deep convolutional neural networks (CNNs) are widely used in feature classification, recommender systems and image recognition. Deep CNNs are difficult to be fully deployed to edge/mobile/IoT devices because of both memory and computation intensive workloads. The energy efficiency of CNNs is dominated by convolution computation and off-chip memory accesses, especially for DRAM accesses. In this tutorial, we will outline the important bottle-necks and solutions for energy-efficient computing hardware of mobile/edge-based AI inference, notably for DRAM accesses. We will then discuss several memory-centric accelerator design approaches and interconnection architectures using advanced technologies, including TSV 3D-SRAM, 3D-DRAM, monolithic 3D-SRAM and computation-in-memory circuits.

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**EFFICIENT POWER DESIGN FOR IOT/IOT & 5G APPLICATIONS**

BRIAN ZAHNSTECHER
POWERROX LLC, USA
10:45AM-12:15PM | SEPT. 8

**Abstract:** Systems-On-Chip (SoC) are increasing in automotive applications like airbag, braking, power steering, and motor drivers. Automotive ICs are similar to conventional analog circuits used in consumer electronics, but they have to handle a wide range of input voltage (5V to 40V) and currents (30mA to 4A) and withstand -18V levels. This tutorial introduces the SoC requirements, design of high side and low side drivers, R-L-C loads, thermal and electrical Safe Operating Area, diagnostics, transceivers, biasing techniques to ensure correct turn ON/OFF behavior, and parasitic bipolars. Finally, the tutorial presents the scalability and programmability of these designs.

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**ANNEALING PROCESSING AND EMERGING NON-VOLATILE MEMORY FOR AI CHIPS**

TAKAYUKI KAWAHARA
TOKYO UNIV. OF SCIENCE, JAPAN
9:00-10:30AM | SEPT. 8

**Abstract:** First, the importance of processing on the edge is outlined. This is followed by a discussion of neural networks and deep learning as part of the development trends of AI chips, after which the incorporation of learning functions, sparseness, and accuracy of calculation is discussed. Next, it moves on to discuss the development trends of emerging nonvolatile memories, especially STT-RAM and SOT-RAM, that are vital for low power consumption and examples of applications to AI. Finally, the development of the fully-coupled-spin annealing AI chip that helps solve combinatorial optimization problems is disclosed. This represents a new paradigm in edge computing.

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**PORTABLE AND SCALABLE HIGH VOLTAGE CIRCUITS FOR AUTOMOTIVE APPLICATIONS IN BICMOS PROCESSES**

SRI NAVANEETH EASWARAN
TEXAS INSTRUMENTS, USA
10:45AM-12:15PM | SEPT. 8

**Abstract:** First, the importance of processing on the edge is outlined. This is followed by a discussion of neural networks and deep learning as part of the development trends of AI chips, after which the incorporation of learning functions, sparseness, and accuracy of calculation is discussed. Next, it moves on to discuss the development trends of emerging nonvolatile memories, especially STT-RAM and SOT-RAM, that are vital for low power consumption and examples of applications to AI. Finally, the development of the fully-coupled-spin annealing AI chip that helps solve combinatorial optimization problems is disclosed. This represents a new paradigm in edge computing.