

21st Annual IEEE International SOCC Conference



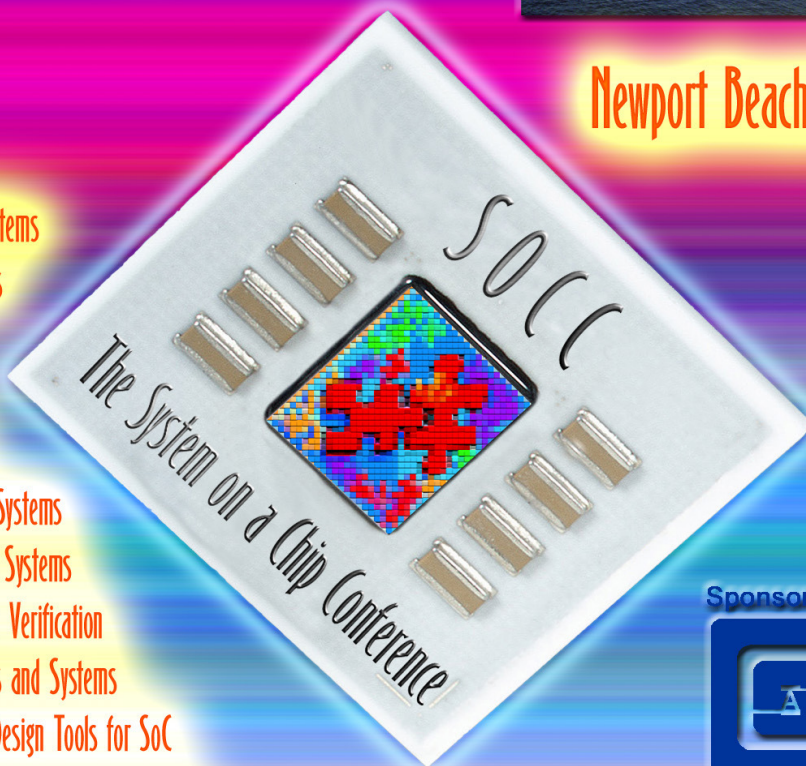
Radisson Hotel

Sept. 17-20, 2008



Newport Beach, CA

- Analog, Mixed-Signal and RF Circuits and Systems
- Embedded Systems, Multi/Many Core Systems
- Embedded Memory Technologies
- Low-Power Circuits, Systems, and Design
- Network on Chip (NoC) and Interconnects
- Digital Signal Processing (DSP) Circuits and Systems
- Video and Multimedia Processing Circuits and Systems
- Signal Integrity, Design for Testability, Design Verification
- Wireline and Wireless Communication Circuits and Systems
- System Level Design Methodology, EDA and Design Tools for SoC
- MEMS/NEMS Devices, Nano-technologies and Design Methodologies
- Reconfigurable and Programmable Circuits and Systems, System on Programmable Devices (FPGAs)



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CONFERENCE-AT-A-GLANCE

Tuesday, Sept. 16		Wednesday, September 17			Thursday, September 18			Friday, September 19			Saturday, September 20			
11:30 a.m. - 5:00 p.m. Tour to NASA Jet Propulsion Lab (JPL)		Registration 7:00 a.m. - 5:00 p.m.			Registration 7:30 a.m. - 5:00 p.m.			Registration 8:00 a.m. - 3:30 p.m.						
		Plenary Session 8:30 a.m. - 11:55 a.m.	Opening Remarks: Thanh Tran, <i>General Conference Chair</i> Technical Program Overview: Thomas Büchner, <i>Technical Program Chair</i> Keynote Presentation: Nick Ilyadis, <i>VP and CTO of Enterprise Networking Group, Broadcom</i> Plenary Presentations: Alexander D. Peleg, <i>Vice President, Mobility Group Director, Intel Architecture Strategic and Platform Planning Intel Corporation</i> Kamran Eshraghian, <i>President, Eshraghian Laboratories Pty Ltd., and Ferrero Family Chair in Electrical Engineering, University of California, Merced.</i>		Technical Sessions 8:30 a.m. - 10:10 a.m.	Track A TA1: Low Power Circuit Design	Track B TB1: Solutions for H.264	Technical Sessions 8:30 a.m. - 10:10 a.m.	Track A FA1: Reconfigurable Computing 1	Track B FB1: Analog and Mixed Signal 2	9:00 a.m. - 12:00 n.	Tutorial Track A SA1 Flying-Adder On-Chip Frequency Synthesis Architecture	Tutorial Track B SB1 Low Power Design under Parameter Variations	Tutorial Track C SC1 Real-time implementation of H.264 video coding
		11:55 a.m. - 1:30 p.m.	Lunch (on your own)			10:30 a.m. - 11:45 a.m.	TA2: Low Power Design Methodologies	TB2: Video Processing	10:30 a.m. - 12:10 p.m.	FA2: Reconfigurable Computing 2	FB2: Analog and Mixed Signal 3	Lunch		
		Technical Sessions 1:30 p.m. - 3:10 p.m.	Track A WA2: Embedded Systems and Multicore Architectures	Track B WB2: System Level Design	Technical Sessions 1:30 p.m. - 3:10 p.m.	Track A TA3: SRAM Memory Technologies	Track B TB3: Analog and Mixed Signal 1	Technical Sessions 1:30 p.m. - 3:10 p.m.	FA3: CAD	FB3: Communication and Processing	12:10 p.m. - 1:30 p.m.	Lunch (on your own)		
		3:30 p.m. - 5:10 p.m.	WA3: Signal Integrity	WB3: Network on Chip	3:30 p.m. - 4:25 p.m.	"Hot Topic" Plenary Presentation: Dynamic Configuration: Beyond Video Coding Standards Iain Richardson, <i>Centre for Video Communications, The Robert Gordon University, UK</i>		Embedded Tutorials 3:30 p.m. - 5:30 p.m.	TFA1: Design and Verification of Complex SoC with Configurable, Extensible Processors	TFB1: A New Generation of C-Base Synthesis Tool and Domain-Specific Computing	1:00 p.m. - 4:00 p.m.	SA2 Understanding and Effectively Suppressing the Noise Coupling in Mixed-Signal SOC Applications	SB2 Asynchronous Circuit Design using Handshake Solutions	
	5:10 p.m. - 6:40 p.m.	Poster Session with Reception			4:30 p.m. - 6:00 p.m.	Panel Discussion								

Wednesday, September 17 - Morning

PLENARY SESSION

8:30 a.m. - 11:55 a.m.

8:30 a.m. - 8:45 a.m.

Opening Remarks: Thanh Tran, *General Conference Chair*

Technical Program Overview: Thomas Büchner, *Technical Program Chair*

	<u>KEYNOTE PRESENTATION:</u>
8:45 a.m. - 9:45 a.m.	<p><i>“SOC Challenges in the Terabit Networks Era”</i> Nick Ilyadis <i>VP and CTO of Enterprise Networking Group, Broadcom</i></p>
9:45 a.m. - 10:05 a.m.	Coffee break
	<u>PLENARY PRESENTATIONS:</u>
10:05 a.m. - 11:00 a.m.	<p><i>“Future Trends in PC Computing and their Implications to SoC”</i> Alexander D. Peleg <i>Vice President, Mobility Group</i> <i>Director, Intel Architecture Strategic and Platform Planning</i> <i>Intel Corporation</i></p>
11:00 a.m. - 11:55 a.m.	<p><i>“Surfing the iSoC Multitechnology Platform: Volumetric Growth beyond Moore's Law”</i> Dr. Kamran Eshraghian <i>President, Eshraghian Laboratories Pty Ltd., and</i> <i>Ferrero Family Chair in Electrical Engineering,</i> <i>University of California, Merced.</i></p>

11:55 a.m. - 1:30 p.m. LUNCH
(on your own)

Wednesday, September 17 - Afternoon

CONCURRENT SESSIONS

1:30 p.m. – 3:10 p.m.

WA2: Embedded Systems and Multicore Architectures

Chair: *Norbert Schuhmann,
Fraunhofer IIS, Germany*
Co-chair:

WB2: System Level Design

Chair: *Emrah Acar, IBM*
Co-chair: *Kaijian Shi, Synopsys*

**WA2.1 Energy-Optimal Signaling and
Ordering of Bits for Area-Constrained
Interconnects**, *Sharath Jayaprakash and
Nihar Mahapatra, Michigan State
University*

**WB2.1 ILP-based Scheme for Timing
Variation-aware Scheduling and
Resource Binding**, *Yibo Chen and Yuan
Xie, Pennsylvania State University*

**WA2.2 A Unified Power
Measurement and Management
Platform for Pipelined MPSoC
Executions**, *Sungkwan Ku, HanSam Jung
and Ki-Seok Chung, Hanyang University,
Korea*

**WB2.2 Exploiting Loop-Level
Parallelism on Multi-Core Architectures
for the WiMAX Physical Layer**, *Ying Yi,
Wei Han, Adam Major, Ahmet T. Erdogan
and Tughrul Arslan, University of
Edinburgh, UK*

**WA2.3 Partitioned Reuse Cache For
Energy-Efficient Soft-Error Protection
of Functional Units**, *Kaushal Gandhi and
Nihar Mahapatra, Michigan State
University*

**WB2.3 Extensible Software Emulator
for Reconfigurable Instruction Cell
Based Processors**, *Mark Muir, Iain
Lindsay and Tughrul Arslan, University of
Edinburgh, UK*

**WA2.4 The Role of Interconnects in
the Performance Scalability of
Multicore Architectures**, *Jiangjiang Liu¹
and Nihar Mahapatra², ¹Lamar University
and ²Michigan State University*

**WB2.4 MRPSIM: A TLM Based
Simulation Tool for MPSoCs Targeting
Dynamically Reconfigurable Processors**,
*Wei Han, Ying Yi, Mark Muir, Ioannis
Nousias, Tughrul Arslan and Ahmet
Erdogan, University of Edinburgh, UK*

3:10 p.m. - 3:30 p.m. COFFEE BREAK

CONCURRENT SESSIONS

3:30 p.m. – 5:10 p.m.

WA3: Signal Integrity

Chair: *Radu Secareanu, Freescale*
Co-chair: *Danella Zhao, UL Lafayette*

WB3: Network on Chip

Chair: *Maurizio Palesi, University of Catania, Italy*
Co-Chair: *Sao-Jie Chen, NTU, Taiwan*

WA3.1 Pseudo-Random Clocking to Enhance Signal Integrity, *Selcuk Kose, Emre Salman, Zeljko Ignjatovic and Eby G. Friedman, University of Rochester*

WB3.1 Fluidity Concept for NoC: A Congestion Avoidance and Relief Routing Scheme, *Ying-Cherng Lan, Michael Chin Chen¹, Alan P. Su², Yu-Hen Hu¹ and Sao-Jie Chen¹, ¹National Taiwan University and ²Springsoft Inc.*

WA3.2 Nanoscale On-Chip Decoupling Capacitors, *Mikhail Popovich and Eby Friedman, University of Rochester*

WB3.2 Configurable Error Correction for Multi-Wire Errors in Switch-to-Switch SoC Links, *Qiaoyan Yu and Paul Ampadu, University of Rochester*

WA3.3 Built-In Functional Tests for Fast Validation of a 40Gbps Coherent Optical Receiver SoC ASIC, *Yuejian Wu, Sandy Thomson, Han Sun, Chandra Bontu and Eric Hall, Nortel*

WB3.3 Guaranteeing QoS with the Pipelined Multi-Channel Central Caching NoC Communication Architecture, *Azeez Sanusi, Nan Wang and Magdy Bayoumi, University of Louisiana at Lafayette*

WA3.4 A Multi-Wire Error Correction Scheme for Reliable and Energy Efficient SoC Links using Hamming Product Codes, *Bo Fu and Paul Ampadu, University of Rochester*

WB3.4 Energy Minimization using a Greedy Randomized Heuristic for the Voltage Assignment Problem in NoC, *Pavel Ghosh and Arunabha Sen, Arizona State University*

5:10 p.m. - 6:40 p.m. POSTER SESSION and RECEPTION BUFFET

POSTER SESSION with Reception

Wednesday, Sept. 17
5:10 p.m. – 6:40 p.m.

Chair: *Thomas Büchner, IBM*
Co-chair: *Andrew Marshall, TI*

- P.1 Composability in the Time-Triggered System-on-Chip Architecture**, *Hermann Kopetz, Christian El Salloum, Bernhard Huber, Roman Obermaisser and Christian Paukovits, Vienna University of Technology, Austria*
- P.2 A Systematic Approach to Synthesis of Verification Test-suites for Modular SoC Designs**, *Sudhakar Surendran¹, Rubin Parekhji¹ and R Govindarajan², ¹Texas Instruments and ²Indian Institute of Science*
- P.3 A 300-mV 36-uW Multiphase Dual Digital Clock Output Generator with Self-Calibration**, *Ming-Hung Chang, Li-Pu Chuang, I-Ming Chang and Wei Hwang, National Chiao-Tung University, Taiwan*
- P.4 A Resistance Deviation-to-Time Interval Converter for Resistive Sensors**, *Ji-Man Park and Sung-ik Jun, ETRI, Korea*
- P.5 Design Methodology for HD Photo Compression Algorithm Targeting a FPGA**, *Seth Groder and Kenneth Hsu, Rochester Institute of Technology*
- P.6 Design of Low Flicker Noise Active CMOS Mixer**, *Shao-Min Hsu, Yuyu Chang and John Choma, University of Southern California*
- P.7 65nm Sub-Threshold 11t-SRAM for Ultra Low Voltage Applications**, *Farshad Moradi¹, Dag T. Wisland¹, Snorre Aunet¹, Hamid Mahmoodi, and Tuan Vu Cao¹, ¹University of Oslo, Norway, and ²San Francisco State University*
- P.8 Evaluation Of Contrast Limited Adaptive Histogram Equalisation (CLAHE) Enhancement on a FPGA**, *Phillip David Ferguson¹, Tughrul Arslan², Ahmet Erdogan² and Andrew Parmley³, ¹Institute Of System Level Integration, ²University of Edinburgh, ³Thales Optronics Ltd.*
- P.9 Novel Start-Up Circuit with Enhanced Power-Up Characteristic for Bandgap References**, *Tuan Vu Cao¹, Dag T. Wisland¹, Tor Sverre Lande¹, Farshad Moradi¹ and Young Hee Kim², ¹University of Oslo, Norway, and ²Changwon National University, South Korea*
- P.10 Unification of Obstacle-Avoiding Rectilinear Steiner Tree Construction**, *Iris Hui-Ru Jiang, Shung-Wei Lin and Yen-Ting Yu, National Chiao Tung University, Taiwan*
- P.11 Analysis of retention time under multi-configuration on a DORGA**, *Daisaku Seto and Minoru Watanabe, Shizuoka University, Japan*

- P.12 Performance Evaluation of a FFT Using Adaptive Clocking**, *Hanni Bagnordi and Mabo Ito, University of British Columbia, Canada*
- P.13 A Comparator-based Switched-capacitor Integrator Using a New Charge Control Circuit**, *Farhad Alibeygi Parsan and Ahmad Ayatollahi, Iran University of Science and Technology*
- P.14 Area Efficient Delay-Insensitive and Differential Current Sensing On-Chip Interconnect**, *Ethiopia Nigussie, Juha Plosila and Jouni Isoaho, Department of Information Technology, University of Turku, Finland*
- P.15 Temperature Measurement in Content Addressable Memory Cells using Bias-Controlled VCO**, *Basab Datta and Wayne Burlison, Electrical & Computer Engineering Department, University of Massachusetts-Amherst*
- P.16 A Coarse-Grained Dynamically Reconfigurable MAC Processor For Power-Sensitive Multi-Standard Devices**, *Syed Waqar Nabi¹, Cade C. Wells¹ and Wim Vanderbauwhede², ¹Institute for System Level Integration and ²University of Glasgow, UK*
- P.17 A Multi-mode Sphere Detector Architecture for WLAN Applications**, *Ramin Shariat-Yazdi and Tad Kwasniewski, Department of Electronics, Carleton University, Canada*
- P.18 Slack Redistribution in Pipelined Circuits for Enhanced Soft-Error Rate Reduction**, *Srivathsan Krishnamohan¹ and Nihar Mahapatra², ¹Synopsys Inc. and ²MSU*
- P.19 Application Development Flow for On-Chip Distributed Architectures**, *Khalid Latif, Moazzam Niazi¹, Tiberiu Seceleanu², Sakir Sezer³ and Hannu Tenhunen¹, ¹University of Turku, Finland, ²ABB Corporate Research, and ³Queens University Belfast, Ireland*
- P.20 A Novel 0.6V CMOS Folded Gilbert-Cell Mixer for UWB Applications**, *Md. Mahbub Reja, Kambiz Moez and Igor Filanovsky, University of Alberta, Canada*

Thursday, September 18 - Morning

CONCURRENT SESSIONS

8:30 a.m. – 10.10 a.m.

TA1: Low Power Circuit Design

Chair: *Sanu Mathew, Intel*
Co-chair: *Yong-Bin Kim, Northeastern University*

TB1: H.264

Chair: *Nagi Naganathan, LSI Corp.*
Co-Chair: *Ken Hsu, RIT*

TA1.1 A Robust Ultra-Low Power Asynchronous FIFO Memory with Self-Adaptive Power Control, *Mu-Tien Chang, Po-Tsang Huang and Wei Hwang, National Chiao Tung University, Taiwan*

TB1.1 Invited Paper: Implementing High Definition Video CODEC on TI DM6467 SoC, *Jian Wang and Gang Hua, Texas Instruments*

TA1.2 A Low Power and Low Area Active Clock Deskewing Technique for sub-90nm technologies, *Ashok Narasimhan and Ramalingam Sridhar, State University of New York at Buffalo*

TB1.2 A 5.46 mW H.264/AVC Video Stream Parser, *Michelle Brown¹ and Kenneth W. Hsu², ¹Intel Corp., and ²Rochester Institute of Technology*

TA1.3 A Low Power 32 Nanometer CMOS Digitally Controlled Oscillator, *Jun Zhao and Yong-Bin Kim, Northeastern University*

TB1.3 A Low-power Design of Quantization for H.264 Video Coding Standard, *Michael Michael and Kenneth Hsu, Rochester Institute of Technology*

TA1.4 Pseudo Parallel Architecture for AES with Error Correction, *YiXin Su and Jimsoon Mathew, University of Bristol, UK*

TB1.4 Speed Control for a Hardware Based H.264/AVC Encoder, *Chae Eun Rhee, Jin-Su Jung and Hyuk-Jae Lee, Seoul National University, Korea*

**10:10 a.m. - 10:30 a.m. COFFEE
BREAK**

Thursday, September 18 – Morning (cont'd)

CONCURRENT SESSIONS

10:30 a.m. – 11:45 a.m.

TA2: Low Power Design Methodologies

Chair: *Yong-Bin Kim,*
Northeastern University
Co-chair: *Sanu Mathew, Intel*

TB2: Video Processing

Chair: *Ken Hsu, RIT*
Co-chair: *Nagi Naganathan, LSI Corp.*

TA2.1 Power Optimization for FinFET-based Circuits Using Genetic Algorithms, *Jin Ouyang and Yuan Xie, Penn State Univ.*

TB2.1 A Multi-Standard Micro-Programmable Deblocking Filter Architecture and its Application to VC-1 Video Decoder, *Ricardo Citro¹, Miguel Guerrero², Jae-Beom Lee³ and Maria Pantoja⁴, ¹Intel Corp., ²Nvidia Corp., ³Sarnoff Corp., and ⁴Santa Clara Univ.*

TA2.2 In-Situ Self-Aware Adaptive Power Control with Multi-Mode Power Gating Network, *Wei-Chih Hsieh and Wei Hwang, National Chiao Tung University, Taiwan*

TB2.2 Multi-Standard Sub-Pixel Interpolation Architecture for Video Motion Estimation, *Liang Lu, John McCanny and Sakir Sezer, Queen's University Belfast, UK*

TA2.3 Supply Voltage Selection in Voltage Island based SoC Design, *Dipanjan Sengupta and Resve Saleh, Univ. Of British Columbia, Canada*

TB2.3 An Efficient Lossless Embedded Compression Engine Using Compacted-FELICS Algorithm, *Yu-Yu Lee, Yu-Hsuan Lee and Tsung-Han Tsai, National Central University, Taiwan*

11:45 a.m. - 1:30 p.m.
LUNCHEON with guest speaker:

David F. Doody,
Flight Operations Lead, Cassini Mission Support & Services, NASA Jet Propulsion Lab
“Cassini-Huygens at Saturn”

Thursday, September 18 - Afternoon

CONCURRENT SESSIONS

1:30 p.m. – 3:10 p.m.

TA3: SRAM Memory Technologies

Chair: *Norbert Schuhmann, Fraunhofer IIS, Germany*
Co-Chair:

TB3: Analog and Mixed-Signal 1

Chair: *Hongjiang Song, Intel*
Co-chair: *Gin-Kou Ma, ITRI*

TA3.1 Low-Power Floating Bitline 8-T SRAM Design with Write Assistant Circuits, *Hao-I Yang, Ssu-Yun Lai and Wei Hwang, National Chiao-Tung University, Taiwan*

TB3.1 1.5V 0.5mW 2MSPS 10b DAC with Rail-to-Rail Output in 0.13 μ m CMOS Technology, *Fuding Ge, Malay Trivedi, Brent Thomas, William Jiang and Hongjiang Song, Intel Corp.*

TA3.2 A Subthreshold Single Ended I/O SRAM Cell Design for Nanometer CMOS Technologies, *Jawar Singh, Jimsoon Mathew and Dhiraj Pradhan, University of Bristol, UK*

TB3.2 Statistical Averaging Based Linearity Optimization for High Speed Converter Architectures in Nanoscale Processes, *Martin Kosakowski¹, Reimund Wittmann¹ and Werner Schardein², ¹Nokia GmbH, and ²Univ. Dortmund, Germany*

TA3.3 Low Power 8-T SRAM Using 32nm Independent Gate FinFET Technology, *Young Bok Kim, Yong-Bin Kim and Fabrizio Lombardi, Northeastern University*

TB3.3 A Higher-Order Mismatch-Shaping Method for Multi-Bit Sigma-Delta Modulators, *Alexendar Lavzin¹, Mucahit Kozak² and Eby Friedman³, ¹Israel Army, ²Intrinsic Corp., and ³Univ. of Rochester*

TA3.4 Failure Analysis for Ultra Low Power Nano-CMOS SRAM Under Process Variations, *Jawar Singh, Jimson Mathew, Dhiraj K. Pradhan and Saraju P. Mohanty, University of Bristol, UK*

TB3.4 A Novel Sub-1 Volt Reference with all CMOS, *Sameer Somvanshi¹, Subash Bose², Sakshi Arora³, and Santosh¹, ¹BITS-Pilani, India, ²CEERI-Pilani, India, and ³Stanford University*

3:10 p.m. - 3:30 p.m. COFFEE BREAK

3:30 p.m. – 4:25 p.m.

“Hot Topic” Plenary Presentation

Iain Richardson

Centre for Video Communications, The Robert Gordon University, UK

“Dynamic Configuration: Beyond Video Coding Standards”

4:30 p.m. – 6:00 p.m.

Panel Discussion

“Ultra-Green Systems-on-Chip -- Hype or reality?”

Friday, September 19 - Morning

CONCURRENT SESSIONS

8:30 a.m. – 10:10 a.m.

FA1: Reconfigurable Computing 1

Chair: *Jürgen Becker, Univ. Karlsruhe, Germany*
 Co-Chair: *Tughrul Arslan, Univ. Edinburgh, UK*

FB1: Analog and Mixed Signal 2

Chair: *Gin-Kou Ma, ITRI*
 Co-chair: *Hongjiang Song, Intel*

FA1.1 Design Space Exploration for Application Specific FPGAs In System-on-a-Chip Designs, *Mark Hammerquist and Roman Lysecky, University of Arizona*

FB1.1 VLSI Passive Switched Capacitor Signal Processing Circuits: Circuit Architecture, Closed Form Modeling and Applications, *Hongjiang Song, Yan Song and Tai-Hua Chen, Intel Corp.*

FA1.2 A Framework of Architectural Synthesis for Dynamically Reconfigurable FPGAs, *Ting Liu, Camel Tanougast and Serge Weber, LIEN, Univ. Nancy, France*

FB1.2 A Novel CMOS Exponential Approximation Circuit, *Ming-Lang Lin¹, Ahmet Erdogan¹, Tughrul Arslan¹ and Adrian Stoica², ¹University of Edinburgh, UK, and ²NASA JPL*

FA1.3 Reconfigurable Multimedia Accelerator for Mobile Systems, *Samar Yazdani¹, Joel Cambonie¹ and Bernard Pottier², ¹STMicroelectronics and ²Université de Bretagne Occidentale, France*

FB1.3 3-D Heterogeneous SoC for Detecting and Filtering Infected Biological Cells, *Vijay Jain, University of South Florida*

FA1.4 Energy Consumption Reduction Mechanism by Tuning Cache Configuration Using NIOS II Processor, *Abel Silva-Filho and Sidney Lima, Universidade de Pernambuco, Brazil*

FB1.4 Novel Mixed Domain VLSI Signal Processing Circuits for High Performance, Low Power and Area Penalty SOC Signal Processing, *Hongjiang Song, Intel Corp.*

10:10 a.m. - 10:30 a.m. COFFEE BREAK

Friday, September 19 – Morning (cont'd)

CONCURRENT SESSIONS

10:30 a.m. – 12:10 a.m.

FA2: Reconfigurable Computing 2

Chair: *Tughrul Arslan, Univ. Edinburgh, UK*
Co-Chair: *Jürgen Becker, Univ. Karlsruhe, Germany*

FB2: Analog and Mixed Signal 3

Chair: *Gin-Kou Ma, ITRI*
Co-Chair: *Hongjiang Song, Intel*

FA2.1 Design of a Baseband Processor for Software Radio Using FPGAs, *Ferney Amaya-Fernández¹ and Jaime Velasco-Medina², ¹Universidad Javeriana, and ²Universidad del Valle, Colombia*

FB2.1 A 6-Gbit/s SATA Spread-Spectrum Clock Generator Using Two-Stage Delta-sigma Modulator, *Hong-Yi Huang, Li-Wei Huang, Wei-Sheng Tseng and Chih-Yuan Hsu, National Taipei University, Taiwan*

FA2.2 OFDM Symbol Timing Synchronization System on a Reconfigurable Instruction Cell Array, *Xin Zhao, Ahmet T. Erdogan and Tughrul Arslan, University of Edinburgh, UK*

FB2.2 A Spread Spectrum Clock Generator Using Digital Modulation Scheme, *Chorng-Sii Hwang¹, Huan-Chun Li² and Hen-Wai Tsao², ¹National Yunlin University of Science and Technology, and ²National Taiwan University, Taiwan*

FA2.3 Reconfigurable Flash A/D Converters, *Cristian Onete, NXP Semiconductors, Netherlands*

FB2.3 All Digital Time-To-Digital Converter Using Single Delay-Locked Loop, *Hong-Yi Huang, Yi-Jui Tsai, Kung-Liang Ho and Chan-Yu Lin, National Taipei University, Taiwan*

FA2.4 Programmable All-digital Adaptive Deskewing and Phase shifting, *Alireza Kaviani, Tao Pi and Declan Kelly, Xilinx Inc*

FB2.4 A New Low Voltage, High PSRR, CMOS Bandgap Voltage Reference, *Seiede Fateme Ashrafi¹, Mohammad Chahardori², and Seied Mojtaba Atarodi², ¹Niro Research Institute, and ²Sharif University of Technology, Iran*

12:10 p.m. - 1:30 p.m. LUNCH (on your own)

Friday, September 19 - Afternoon**CONCURRENT SESSIONS**

1:30 p.m. – 3:10 p.m.

FA3: CAD

Chair: *Kaijian Shi, Synopsys*
Co-Chair: *Emrah Acar, IBM*

FA3.1 A Timing Methodology Considering Within-Die Clock Skew Variations, *Savithri Sundareswaran¹, Sergey Gavrilov², Roman Soloviev², Rajendran Panda¹, Lucie Nechanicka¹ and Jacob Abraham³, ¹Freescale Inc., ²IPPM, Russia, and ³University of Texas at Austin*

FA3.2 X-Clock Routing Based on Pattern Matching, *Chia-Chun Tsai¹, Chung-Chieh Kuo², Jan-Ou Wu³, Trong-Yen Lee² and Rong-Shue Hsiao², ¹Nanhua University, ²National Taipei University, and ³De Lin Institute of Technology, Taiwan*

FA3.3 An Automated Design Method for Chip Power Distribution, *Di Phan, Chris Berry, Frank Malgioglio and Alan Wagstaff, IBM Corp.*

FB3: Communication and Processing

Chair: *Mark Schrader, Harris*
Co-chair: *Gerd Ascheid, Aachen Univ. of Techn., Germany*

FB3.1 A Low Power 1-Gbps Reconfigurable LDPC Decoder Design for Multiple 4G Wireless Standards, *Yang Sun and Joseph Cavallaro, Rice University*

FB3.2 High Performance IP Lookup Circuit Using DDR SDRAM, *Xin Yang¹, Jun Mu¹, Sakir Sezer¹, John McCanny¹ and Earl Swartzlander², ¹Queen's University Belfast, UK, and ²Univ. of Texas at Austin*

FB3.3 Power/Throughput/Area Efficient PIM-based Reconfigurable Array for Parallel Processing, *Martin Margala¹, Sohan Purohit¹, Sai Chalamalasetti¹ and Pasquale Corsonello², ¹University of Massachusetts Lowell, ²University of Calabria, Italy*

FB3.4 A Discrepancy Computationless RiBM Algorithm and Its Architecture for BCH Decoders, *Sangho Yoon and Hanho Lee, Inha University, Korea*

**3:10 p.m. - 3:30 p.m. COFFEE
BREAK**

Friday, September 19 – Afternoon (cont'd)

CONCURRENT EMBEDDED TUTORIALS

3:30pm – 5:30 p.m.

Chair: Kaijian Shi, *Synopsys*

	Tutorial Track A	Tutorial Track B
3:30 p.m. - 5:30 p.m.	TFA1 Design and Verification of Complex SoC with Configurable, Extensible Processors Steve Leibson and Grant Martin, <i>Tensilica, Inc.</i>	TFB1 A New Generation of C-Base Synthesis Tool and Domain-Specific Computing Zhiru Zhang, <i>AutoESL Design Technologies, Inc.</i>



TUTORIAL WORKSHOPS

Saturday, Sept. 20, 2008
8:30 a.m. - 4:20 p.m.

Saturday, September 20			
Morning Workshops	Tutorial Track A	Tutorial Track B	Tutorial Track C
8:30 a.m. - 10:00 a.m.	SA1 Flying-Adder On-Chip Frequency Synthesis Architecture Liming Xiu, <i>Texas Instruments</i>	SB1 Low Power Design under Parameter Variations Swarup Bhunia, <i>Case Western Reserve University</i> , and Kaushik Roy, <i>Purdue University</i>	SC1 Real-time implementation of H.264 video coding Iain Richardson, <i>Centre for Video Communications, The Robert Gordon University, UK</i>
10:00 a.m. - 10:20 a.m.	Coffee break		
10:20 a.m. - 11:50 a.m.	SA1 Flying-Adder On-Chip Frequency Synthesis Architecture Liming Xiu, <i>Texas Instruments</i>	SB1 Low Power Design under Parameter Variations Swarup Bhunia, <i>Case Western Reserve University</i> , and Kaushik Roy, <i>Purdue University</i>	SC1 Real-time implementation of H.264 video coding Iain Richardson, <i>Centre for Video Communications, The Robert Gordon University, UK</i>
11:50 a.m. - 1:00 p.m.	LUNCH*		
Afternoon Workshops 1:00 p.m. - 2:30 p.m.	SA2 Understanding and Effectively Suppressing the Noise Coupling in Mixed-Signal SOC Applications Cosmin Iorga, <i>Noisecoupling.com</i>	SB2 Asynchronous Circuit Design using Handshake Solutions Ad Peeters and Mark de Wit, <i>Handshake Solutions</i>	
2:30 p.m. - 2:50 p.m.	Coffee break		
2:50 p.m. - 4:20 p.m.	SA2 Understanding and Effectively Suppressing the Noise Coupling in Mixed-Signal SOC Applications Cosmin Iorga, <i>Noisecoupling.com</i>	SB2 Asynchronous Circuit Design using Handshake Solutions Ad Peeters and Mark de Wit, <i>Handshake Solutions</i>	

*Lunch not included in student registration

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Check all that apply:

- Author - Session No: _____ Workshop Presenter

NOTE FOR AUTHORS: Each paper is required to have at least one full registration from one of the authors by August 15, 2008; student registration will not be counted towards this requirement! If you are an author and this registration counts towards this requirement please state the paper number above.

GUIDED TOUR TO NASA JPL

TUESDAY, September 16 (ca. 11:30am – 5pm)

Number of Participants: _____

(Please enter full name and citizenship for each participant)

LAST NAME FIRST NAME(S) CITIZENSHIP

Note: tour registration is only possible until August 15 !

PAYMENT

Registration Fee \$ _____

Tutorial Workshops \$ _____

Addl. Banquet \$ _____

Addl. Proceedings \$ _____

JPL Tour \$ _____

TOTAL REMITTANCE \$ _____

<i>CONFERENCE FEES</i>	Before Aug. 31	After Aug. 31
IEEE Member - Full Conference	<input type="checkbox"/> \$450	<input type="checkbox"/> \$500
Non-Member - Full Conference	<input type="checkbox"/> \$500	<input type="checkbox"/> \$550
Full Time Student (ID required)	<input type="checkbox"/> \$150	<input type="checkbox"/> \$150
Addl. Luncheon Ticket	<input type="checkbox"/> \$35	<input type="checkbox"/> \$35
<i>WORKSHOP (two half day tutorials; select below)</i>		
IEEE Member	<input type="checkbox"/> \$250	<input type="checkbox"/> \$275
Non-Member	<input type="checkbox"/> \$250	<input type="checkbox"/> \$275
Full Time Student	<input type="checkbox"/> \$75	<input type="checkbox"/> \$75
<i>One half day tutorial; select below</i>		
IEEE Member – ½ day	<input type="checkbox"/> \$100	<input type="checkbox"/> \$125
Non-Member – ½ day	<input type="checkbox"/> \$100	<input type="checkbox"/> \$125
Full Time Student – ½ day	<input type="checkbox"/> \$40	<input type="checkbox"/> \$40
EXTRA 2008 PROCEEDINGS		
IEEE Member	<input type="checkbox"/> \$75	
Non-member	<input type="checkbox"/> \$85	
By mail – add per book	<input type="checkbox"/> \$25	
JPL Tour – Tuesday, Sept.16 –MUST REGISTER BY AUG.15		
Transportation & box lunch	<input type="checkbox"/> \$25	

Please mail or fax this form to:
IEEE SOC Conference
19803 Laurel Valley Place
Montgomery Village, MD 20866
Phone: +1-301-527-0900, x104
Fax: +1-301-527-0994

TUTORIAL WORKSHOPS: MARK selected session(s)

SATURDAY, September 20

Morning Workshops (9 am – 12 noon)

- SA1 SB1 SC1 (Choose only one)

Afternoon Workshop (1pm – 4 pm)

- SA2 SB2 (Choose only one)

Payment for registration may be made by check - payable to **SOC Conference** (U.S. Dollars on a U.S. bank) or credit card.

Payment method: MasterCard Visa Check

Credit Card Account Number

Expiration Date _____

HOTEL RESERVATIONS

A block of rooms has been reserved at the Radisson Hotel Newport Beach at a discounted rate of US\$ 141.00 per night plus tax.

Contact the hotel directly at the address below and identify yourself as an IEEE SOC Conference participant to receive the special room rate.

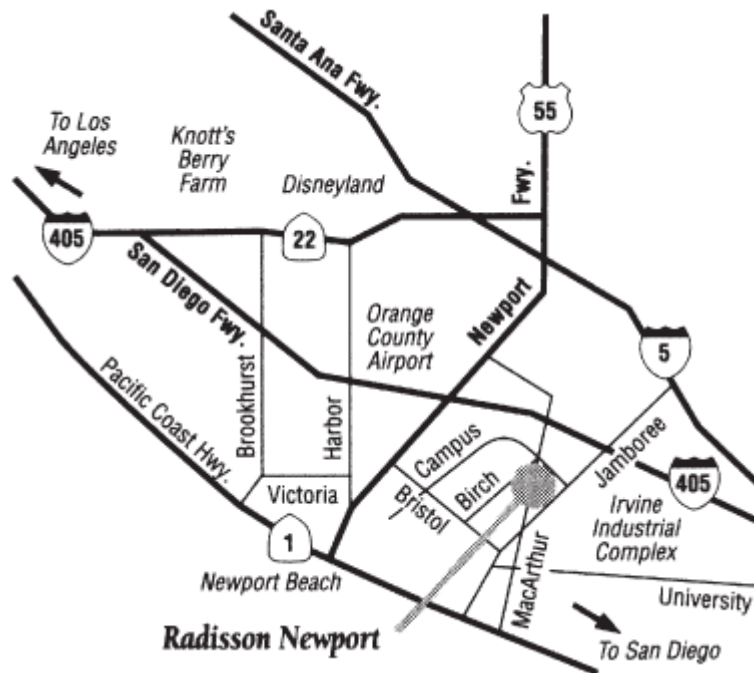
HOTEL ADDRESS:

[The Radisson Hotel Newport Beach](#)

4545 MacArthur Blvd.
Newport Beach, CA 92660
Phone: +1-949-833-0570 or toll free +1-800-333-3333
Fax: +1-949-833-3927
Email: Info@RadissonNewportBeach.com

HOW TO GET THERE:

The Radisson Hotel Newport Beach is centrally located in Orange County close to the business districts of Irvine, Santa Ana, Costa Mesa and Huntington Beach. Just 1/2 mile from the OC/John Wayne Airport, and a FREE shuttle ride away. About 42 miles from Los Angeles Int'l Airport



From I-405 Take the MacArthur Blvd Exit
Turn Left at off ramp
Go 6 Blocks to Birch
Hotel is on the Corner of Birch and Mac Arthur Blvd

Guided Tour at NASA JPL:

We are pleased to be able to offer a guided tour at [NASA Jet Propulsion Lab](#) in Pasadena. The tour will leave at the hotel on Sep. 16, 2008, 11:30 a.m. Bus transportation and box lunch are included in the tour fee of \$25 (see registration form). After arriving at JPL, starting at 1 p.m. you will receive a guided tour of JPL lasting 2-2.5 hours in duration, including a multi-media presentation entitled "Spirit of Exploration," which provides an overview of the Laboratory's activities and accomplishments. Guests may also visit the von Karman Visitor Center, the Space Flight Operations Facility, and the In-Situ Instruments Laboratory.

All adults must bring proper government issued photo ID's (for US citizens that means DL, State ID, Military ID or passport; for foreign nationals you will need either a Greencard or passport).

We suggest everyone wear comfortable shoes as there is a lot of walking on the tour, dress appropriate for the weather. Cameras and video recorders are allowed so feel free to bring them.

We will be back at the hotel around 5:00 p.m.

Please note that you have to **register for the tour with your full name and citizenship by 8/15.**

We have to send a list of all participants to JPL one month ahead of the tour and people not on the list will not be admitted. There will be no late or on-site registration available for the tour.

